NOVATEL'S GPS RECEIVER
THE HIGH PERFORMANCE OEM SENSOR OF THE FUTURE

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Abstract

In this paper, the 10 channel NovAtel GPSCard receiver is presented. This receiver is available as a low cost, high performance GPS sensor, providing features and capabilities to support all OEM applications. NovAtel, a cellular systems and subscriber equipment manufacturer located in Calgary, has developed a completely new GPS receiver from the ground up. Incorporated within the design are advanced technologies at each major component stage, including: the antenna, the RF downconverter and LNA, the ASIC Signal Processor, the CPU, and the software configurable interfaces. This receiver has 10 dedicated channels and is capable of extremely accurate C/A code and L1 carrier phase tracking. The patented C/A code tracking scheme, which uses a wide bandwidth multiple bit sampling method (capable of P code accuracy), is described. NovAtel's GPS sensor also has the ability to output both raw and final position data at rates suitable for even the most demanding applications.

Introduction

The NovAtel GPSCard receiver is a high-performance 10 channel receiver capable of independently tracking the C/A code and carrier phase of all GPS satellites in view. The wide bandwidth RF front end, combined with high rate multi-bit sampling and digital signal processing features, yields substantially higher interference immunity and code phase tracking accuracy. The high performance CPU, with integrated math coprocessor, permits rapid data and position update rates. The dual serial data ports and the assorted input/output strobes provide support for integration with external systems, real-time differential positioning, remote receiver control, data logging, and time transfer.

After a brief overview of the main receiver components, details regarding the design advantages and capabilities of the signal

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processing chip are given. Both simulated and actual satellite code tracking results are presented along with a brief description of the signal correlation methodology.

GPS Receiver Description

The GPS receiver is comprised of an Antenna, LNA, RF/IF section, Signal Processor, CPU and Interface section. Descriptions of these components are contained in the following sections.

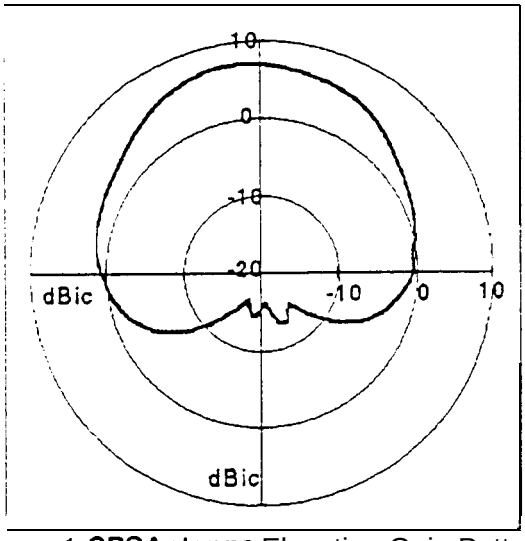

Figure 1-GPSAntenna Elevation Gain Pattern

Antenna The NovAtel GPSAntenna is manufactured using a unique molding and metalizing technique to form the internal radiator element. This design provides the GPS signal reception advantages of a microstrip antenna (i.e. narrow bandwidth, low cost, and ease of assembly), without suffering some of the inherent disadvantages such as cross polarization signal reception, and poor low elevation angle gain (cf. Figure 1). The GPSAntenna's design provides superior polarization which results in cross polarization reception of less than -10 dBic, which effectively reduces unwanted signal reflections. The substrate material used in the antenna element is low loss, with very consistent dielectric properties and excellent high temperature stability.

LNA As shown in Figure 2, the low noise amplifier consists of an RF filter, low noise amplifier stage and buffer amplifier stage. The filter provides rejection for co-located cellular radio, MSAT and Inmarsat transmitters, as well as rejection of image and sub-harmonic frequency signals. The amplifier stages use bipolar devices which maximize reliability, improve unit to unit performance consistency, and minimize cost. The buffer allows the antenna and remaining receiver circuitry to be separated by up to 100 ft. using RG-213 cable. All components including the filter are surface mount devices, resulting in a small circuit area (approximately 1.5 sq. in.), and allowing board assembly using automated manufacturing techniques. The power consumption of the LNA is typically 15 mA at 4.5 VDC.

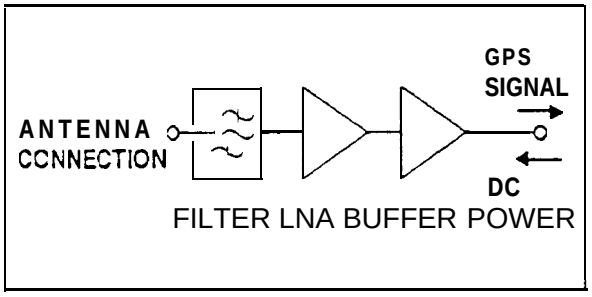

Figure 2 - LNA Block Diagram

RF/IF Figure 3 illustrates the major RF/IF circuits on the GPS receiver board. The high frequency sampling techniques used in the A/D allow a single stage RF to IF downconversion scheme to be used. The input GPS RF signal is filtered and amplified at RF, mixed down to an IF, channel filtered and again amplified before passing the signal to the subsequent A/D stage. Surface mount bipolar technology is used throughout, which results in a circuit area of about 7 1/2 sq. in. The power requirements are in the order of 150 mA at 5 VDC.

As with the LNA, the input filter provides additional filtering for interference signals. Bipolar amplifier stages preamplify and feed the RF signal to a MMIC mixer stage. The mixer receives a synthesized LO signal at about 1540 MHz. The LO is created using a single chip synthesizer, and subsequent frequency doubler. Following the mixer, is a SAW IF filter. This filter is compact, has near ideal brick wall frequency cutoff, and linear phase response. After the IF fitter is an AGC circuit which provides gain compensation for variable cable losses between the antenna and the receiver board, as well as gain variations within the RF sections of the receiver. The AGC also allows the post signal processing stages to optimize the signal level input for the analog to digital (A/D) stage. Amplifiers follow the AGC to bring the signal level up

to that necessary for the A/D. In total, about 100 dB of linear gain is distributed between the RF and IF stages.

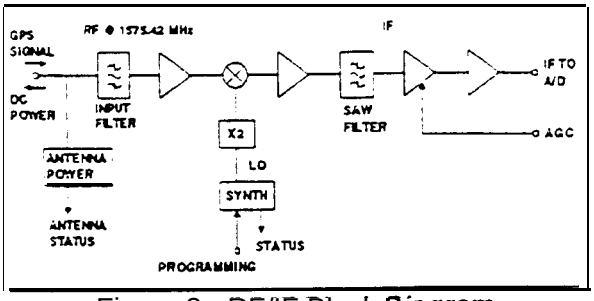

Figure 3 - RF/IF Block Diagram

Built-in-test capability is included to allow for checking of synthesizer integrity and an open/shorted antenna connection. Current limiting circuits are also in place to ensure the receiver is not damaged if the antenna is accidently shorted. The RF section is completely shielded to operate properly in high interference environments.

Signal Processor The Signal Processor is a custom gate array ASIC. This was designed using a sub-micron CMOS process. It consists of 5 independent receiver channels, each capable of very accurate tracking of the code and carrier phase of a GPS satellite.

The GPS signal (plus noise) enters the ASIC in a multibit digital format from the off-chip A/D converter. Multibit and high rate sampling (≈20 MHz) minimize quantization loss to 0.1 dB. The signal is digitized using an IF sampling technique that provides the sequence I, Q, -I, -Q, I, Q ...) where the I and Q in-phase and quadraphase samples are in quadrature. The I and Q data paths are split into individual I and Q channels for sign inversion and processing.

In the INPUT section of the chip (see Figure 4), a histogram of the magnitude of the signal is built up. This information is used by the CPU to adjust the gain of the AGC amplifier in the IF section. This histogram is used to detect the presence of narrowband interference, a unique feature of the Signal Processor. The AGC is normally adjusted to optimize the location of the digitization thresholds. If narrowband interference is detected, the AGC is adjusted to minimize its effect. Output of the INPUT section is sent simultaneously to 5 independent channels.

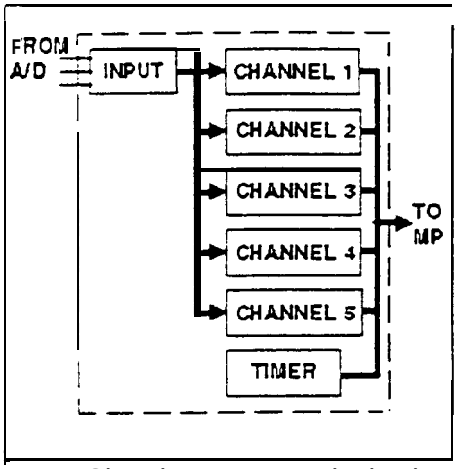

Figure 4 - Signal Processor Block Diagram

Each channel (see Figure 5) consists of a code generator, a phase generator, and two correlators. The code generator provides the C/A code at the correct code frequency. The phase generator consists of a long chain of counters which simultaneously track the carrier and code phases of the received signal. It also generates the early, punctual, and late clocks for the C/A code shift register, which in turn outputs the early, punctual, and late C/A codes. Code phase generation is effectively aided by carrier phase tracking in hardware by appropriate scaling of the carrier Doppler clock.

Two correlators mix the appropriately delayed code with the incoming I and Q samples. The use of these two correlators is described below under the description of the Delay Lock Loop discriminator design. The correlated I and Q samples are subsequently accumulated over either 0.25 or 1 msec.

The TIMER is used to provide a very accurate time source against which all pseudorange and carrier phase measurements are made. Pseudorange measurements are in the form of "Received Time-of-Week". They can be programmed to occur at one of five time intervals - 1 second, 100 msec, 1 msec or at some externally determined rate. When a pseudorange measurement is made, the contents of the phase generator are clocked into output registers simultaneously in all channels. The event is time tagged with the contents of the timer counters, which have also been loaded into output registers. Upon completion, the CPU is supplied

with an interrupt.

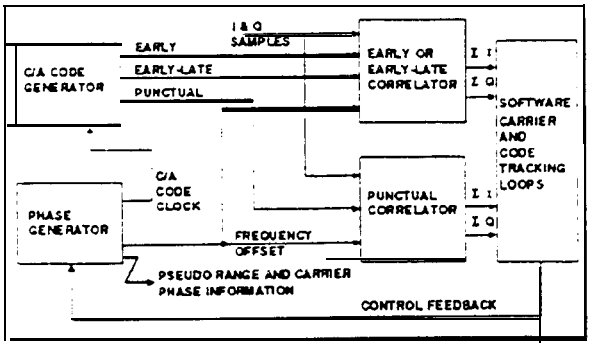

Figure 5 - Channel Block Diagram

The Signal Processor is designed to be cascadeable. That is, appropriate connection features are available so that one can be a master to the others, which operate as slaves. In this way, the processors are synchronized together, eliminating interchannel pseudorange and carrier phase measurement biases.

The ASIC also has the ability to generate an accurate programmable pulse train from 156 Hz to 10.23 MHz. This feature could be used to phase lock the on board TCXO to an external frequency reference. It can also be used to provide non-corrected timing pulses, whose time error is available from the CPU.

CPU The CPU used in the NovAtel GPSCard receiver, is a 20 MHz high performance Inmos T805 32 bit microprocessor with built-in math coprocessor (see Figure 6). There are 4 kilobytes of on-chip high speed RAM and 1 Mbyte of external SRAM.

On the GPSCard development platform, receiver software is stored using on-board volatile memory which must be reloaded each time the receiver is powered up. This is accomplished with a high speed (20 Mbits/sec) serial link through the PC's I/O bus. Programmable Logic Array circuitry, in conjunction with a UART, convert the serial link to the parallel format of the PC's 8 bit ISA bus. Receiver power is also obtained from the PC bus connector.

A Programmable Logic Array is used to demultiplex the address/data bus by latching the addresses into a separate address bus. This same PLA also generates the rest of the control logic for the receiver. This includes the chip selects for the SRAM, the Dual Universal Asynchronus Receiver Transmitter (DUART), the Signal Processors, as well as the control lines to program the local oscillator synthesizer in the RF section. Status signals from the RF section are fed back to the CPU through the PLA.

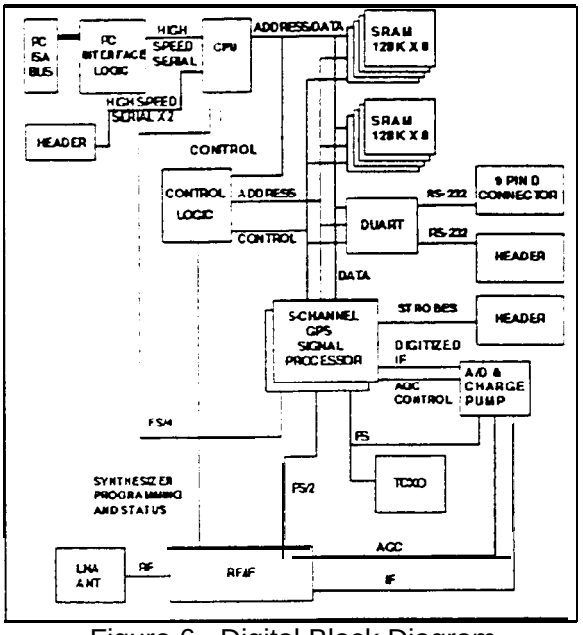

Figure 6 - Digital Block Diagram

The CPU communicates with a pair of 5 channel Signal Processor chips. Each of these Signal Processors accepts the IF signal digitized to multibit resolution. One of the Signal Processors controls a charge pump which varies the gain of the IF amplifier (AGC).

Strobes A strobe header provides a MARK-IN which can be used to request a set of pseudo ranges at the time of the signal, and a MARK-OUT, which will indicate the time a set of ranges was measured by the Signal Processor. Additionally, a 1PPS and a programmable variable frequency are provided at this connector. A fail-safe signal that indicates the receiver is providing valid positions is also available.

Interfaces For off-board communication, two full-duplex RS232 serial channels are provided. The CPU communicates with these serial channels through a DUART. The CPU has two additional high speed serial channels available on the chip which are brought to a header. These channels are capable of 5, 10 or 20 MBits per second and use a proprietary communications format, as opposed to a universal format.

Theory Behind High Pseudorange Accuracy

The accuracy of a pseudorange measurement is proportional to the accuracy that we can position the local C/A code generator to match the incoming C/A code signal. The C/A code signal generated in the GPS satellite is a square digital pulse stream with relatively sharp transitions. As it leaves the satellite, it is bandpass filtered (≈20.46 MHz) to eliminate out-of-band signals (cf. [ICD-GPS-200]). Upon entering the user equipment, it is again bandpass filtered to reject out-of-band signals, as well as reduce the digital signal processing requirements. Figure 7 shows the effect of bandpass filters on a C/A bit. We see that the narrower the filter becomes, the smoother the transitions of the C/A code become. Without sharp transitions, it is very difficult to determine exactly where the transition is, and the less accurate the pseudorange estimate becomes. The sharper the transitions of the incoming C/A code signal are, the sharper the peak of the correlation function becomes with respect to the locally generated C/A code signal.

Pseudorange Accuracy The formula for estimating the accuracy of a pseudorange observable for an early-minus-late power discriminator is as follows:

$$\sigma_\tau = \sqrt{\frac{B_L d}{2\frac{S}{N_0}}\left(1 + \frac{2}{\frac{S}{N_0}T(2-d)}\right)} \text{ chips} \qquad (1)$$

where B_L is bandwidth in Hz of the code tracking loop (delay lock loop - DLL), d is the separation between the early and late correlators (chips), S/N_0 is signal-to-noise density in a 1 Hz bandwidth in ratio-Hz, and T is the predetection integration interval (PDI) of a discriminator sample (for NovAtel, the steady state I/T = 50 Hz).

From Equation 1, we see the accuracy is directly proportional to the square root of $B_L d$ and inversely proportional to the square root of S/N_0. The other factor in the equation is due to noise squaring loss and is negligible at normal operating conditions, where $C/N_0 > 40$ dB-Hz. In order to minimize σ_τ, we must examine carefully all the other parameters.

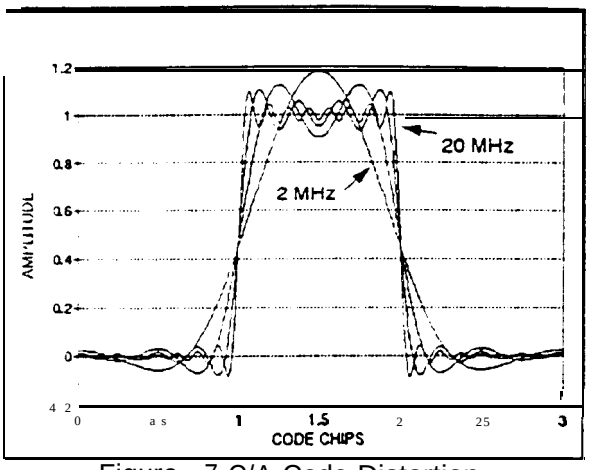

Figure - 7 C/A Code Distortion

Code Tracking Bandwidth The code tracking bandwidth B_L, must be wide enough to track the motion of the received code as it changes with respect to the hardware code generator. In our design, the C/A code generator is controlled in hardware by the carrier phase tracking numerically controlled oscillator (NCO), which is in turn controlled by a phase lock loop. Assuming that the carrier tracking loop does not slip, the code generator is automatically adjusted for the dynamics of the satellite and the receiver. The carrier tracking system effectively removes any apparent dynamic motion from the code loop. The code tracking loop must then only track the divergence between the carrier and the code.

Carrier and code divergence is caused by natural phenomena such as the ionosphere and multipath, as well as unnatural causes such as cycle slips in the carrier tracking loop. Cycle slipping is detected almost instantaneously by the parii check. Multipath effects can be limited by good antenna design and site planning. In the absence of cycle slips, the B_L need only be wide enough for tracking the ionospheric divergence and multipath effects. Initial loop pull-in and stabilization is also a consideration. However, wider bandwidths are used during that period. A bandwidth of 1/30 to 1/20 Hz was chosen for our receiver, configured in a second order loop, i.e. wide enough to track the divergence yet narrow enough to provide good range accuracy. With this bandwidth, the initial acquisition transients in the loop are very low by the time the ephemeris data has been gathered (< 30 seconds).

Signal Strenath Considerations The signal-to noise-ratio is limited by the antenna design, receiver noise figure, filtering losses, and digital processing quantization losses. It is also limited by the broadcast levels of the satellites. Throughout 'he NovAtel GPS receiver design process, a very high priority was focused on low noise. The total noise figure for the entire system from the antenna down to the CPU is 3 dB. This results from a noise figure of 2.7 from the antenna/RF section and 0.3 dB quantization loss from both the A/D and the multibit complex mixers in the correlators. The typical operating GPS signal strength levels obtained from our receiver were C/N_0 values between 45 and 50 dB-Hz. These levels were derived from actual data collected from the roof of NovAtel (30 m. from the antenna field of an 800 MHz cellular base station).

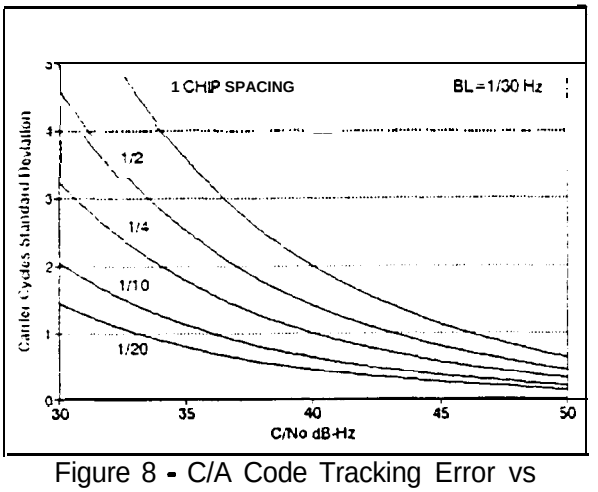

Figure 8 - C/A Code Tracking Error vs Correlator Spacing

Correlator Spacing (d) This is the area where we focused our major design efforts. From Figure 8, which is based on the evaluation of Equation 1, we see the expected C/A code tracking error (converted to L1 carrier cycles) as a function of correlator spacing and signal-to-noise density. The figure illustrates that it is theoretically possible to produce sub-wavelength accuracy (in pseudo range measurements) in the presence of normal C/N_0 (≈ 40 dB-Hz), by narrowing the early/late correlator spacing to below 0.2 chips. The key reason for accuracy improvement with narrower spacing is the fact that the early and late noise contributions are correlated proportional to l-d. Thus, they tend to cancel in the discriminator.

The NovAtel receiver has a tracking channel where the correlator spacing can be adjusted (by software control) from a 1 chip level that is necessary for sky search, down to 0.05 chip spacing for high accuracy tracking. This feature theoretically improves the accuracy by a factor of 4.5 ($\sqrt{20}$) over a conventional C/A code receiver with 1 chip spacing. In fact, it improves the accuracy to within a factor of 1.58 ($10/\sqrt{40}$) of a conventional P code receiver with the same loop bandwidth and with 1 P-chip spacing, accounting for the extra 3 dB of signal strength.

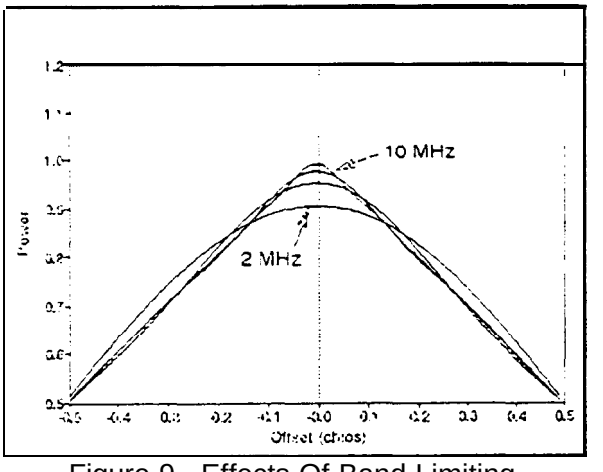

Figure 9 - Effects Of Band Limiting Correlation Power

Bandwidth Considerations In order to achieve this accuracy, however, many features had to be added to the receiver design. To take advantage of the narrow correlator spacing, it is necessary to sharpen up the auto correlation function or peak, so that the correlators are still operating in the linear range of the discriminator. We see from Figure 9 that the top of the correlation peak becomes rounded and loses its linearity as the precorrelation bandwidth is narrowed. The sharper the peak, the closer the conelators can be positioned to it, thus the range estimate becomes more accurate. The minimum spacing of the correlators is limited by the slope of the correlation peak. Figure 10 shows the effect of band limiting on the slope of the correlation peak. It also shows the practical minimum limit of the positioning of the correlators as a function of precorrelation bandwidth.

Sampling Considerations The penalty for opening up the precorrelation bandwidth is the flood of noise that accompanies the signal. It re-

quires that the digital signal processing satisfy the Nyquist theorem, and sample the signal at greater than twice the bandwidth (quadrature sampling). This in turn leads to higher digital processing loads, requiring a GPS digital processing chip with significantly more gates than would normally be necessary for a lower performance receiver. These gates are required to provide pipe-lined NCO's and look ahead counters as well as wider CPU bus bandwidth. The correlation technique also draws more power than a C/A code receiver operating at 2 MHz bandwidth.

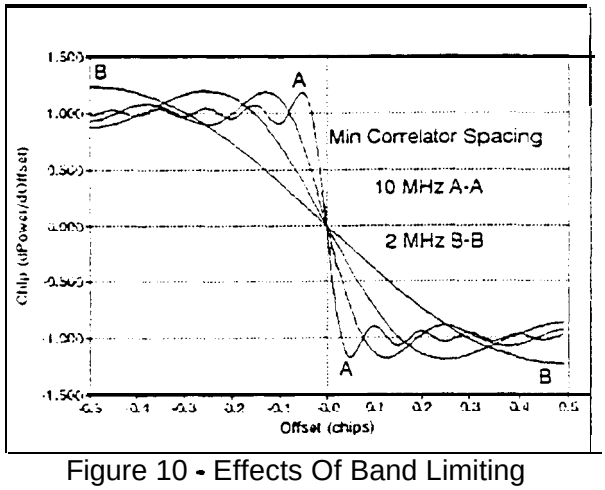

Figure 10 - Effects Of Band Limiting Correlation Slope

Delay Lock Loop Discriminator Design

Hardware Considerations The Signal Processor has the capability of performing code correlation in two different modes: an early-minus-late power mode, and a dot-product mode. The Signal Processor which has two correlators in each channel, can operate one of the correlators as either an early correlator, or an early-minus-late correlator. This feature is illustrated as a functional block diagram in Figure 11. In the early-minus-late power mode, the second correlator operates as a late correlator. In the dot-product mode, the second correlator operates as a punctual (or prompt) correlator. In either case, each correlator includes an in-phase (I) and a quadraphase (Q) sub-channel. The spacing between the correlators can be selected over a range of 1/20 to 1 C/A chip by selecting the clocking of the EPL shift register.

The two modes provide for an implementation of two different types of DLL discriminators for measuring code tracking error: a Dot-Product (DP) discriminator, and an Early-Power-Minus-Late-Power (EL) discriminator. A description of these discriminators is given below, along with their advantages and disadvantages.

The discriminators described are implemented as "normalized" discriminators. That is, they are divided by a power measurement computed from I and Q samples measured over the same time interval. The effect of this normalization is threefold:

1) It eliminates the need for a post-correlation Automatic Gain Control (AGC). This is consistent with the various carrier tracking loops implemented in the receiver that also use normalized carrier phase or frequency discriminators.

2) Normalization effectively suppresses pulse interference effects.

3) Normalization provides a constant discriminator gain over moderate to high signal-to-noise conditions. This is helpful in defining tracking loop gains, and for performing some necessary open loop compensation for accurate measurement processing.

Normalized Dot-Product DLL Discriminator
The normalized DP discriminator is of the form:

$$d\tau = \frac{I_{e-l}I_p + Q_{e-l}Q_p}{I_p^2 + Q_p^2} \qquad (2)$$

where the I and Q values are summed over the appropriate predetection integration interval (PDI). I_{e-l} and Q_{e-l} represent the I and Q values when the hardware is implemented in the dot-product mode. That is, the early-minus-late correlator correlates the incoming signal with the difference between the locally generated code and itself, which is delayed by a predefined conelator spacing. The subscript p represents punctual I and Q, which are the same ones used in the carrier loop discriminators, lock detectors and $\frac{C}{N_0}$ estimator. In this case, the minimum correlator spacing between the early and late correlators is 0.1 C/A chip. Because there is a

punctual code available using this DP discriminator, it provides an advantage for carrier tracking, especially with larger correlator spacings.

The hardware implementation used to generate I_{e-l}, Q_{e-l}, I_p and Q_p is illustrated in Figure 11.

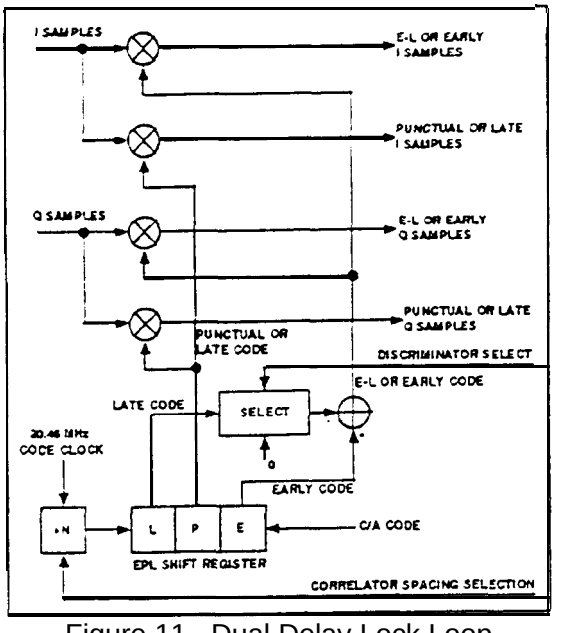

Figure 11 - Dual Delay Lock Loop Discriminator Hardware Implementation

Normalized Early-Power-Minus-Late-Power

The normalized EL discriminator is of the form

$$d\tau = \frac{I_e^2 + Q_e^2 - I_l^2 - Q_l^2}{I_e^2 + Q_e^2 + I_l^2 + Q_l^2} \qquad (3)$$

where the I and Q values are summed over the appropriate predetection integration interval. I_e, If, Q_e and Q_l represent the I and Q values when the hardware is implemented in the early-minus-late power mode. In this case, the carrier loop discriminators, lock detectors, and C/N_0 estimator would use either the early or late samples to replace the punctual I and Q values. The minimum correlator spacing in this mode is 0.05 C/A chips between the early and late correlators, one-half the 20.46 MHz clock period, and one-half of what it is in the DP mode. In this case, the receiver tracks the code with an offset of 0.025 C/A chip. However, if the same procedure is used on all satellites, that offset simply becomes part of the clock solution. We account for it by doing an accurate time transfer. It does represent about 24 nanoseconds.

This EL discriminator has the advantage of the narrower correlator spacing, and thus is used for steady state tracking. The DP discriminator is used for initial tracking loop pull-in, using larger correlator spacings.

The hardware generation of the Ie, If, Q_e and Q_l is illustrated in Figure 11, which is only a slightly different mode of operation than that for the DP discriminator.

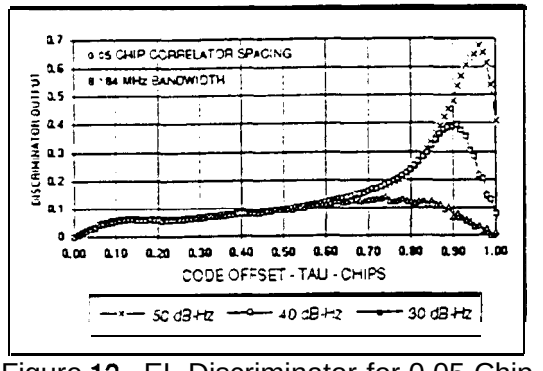

Figure 12 - EL Discriminator for 0.05 Chip Spacing

Theoretical and Simulated DLL Discriminator Performance

For an infinite precorrelation bandwidth, the normalized EL discriminator theoretically has an output at high signal-to-noise ratio of:

$$E(d\tau) = \frac{4(2-d)\tau}{(2-d)^2 + 4\tau^2} \text{ chips}, \quad -\frac{d}{2} \le \tau \le \frac{d}{2} \qquad (4)$$

for smaller tracking errors of τ and early/late correlator spacing d in chips. Of course, narrow precorrelation bandwidths and noise suppression will after this relationship. Because of these effects, Monte Carlo simulations were used to determine the actual characteristics of this discriminator as a function of bandwidth and noise suppression. The expected value of this EL discriminator with 0.05 chip spacing, and its one sigma value, are plotted in Figure 12 for C/N_0 values of 30, 40 and 50 dB-Hz, for which the noise suppression is obviously negligible except at large values of τ. At these large values, when

the tracking error is at the edge of the correlation peak, the normalization effects cause a peak in the discriminator, which could prevent loss of lock. However, the signal-to-noise ratio at those tracking offsets is so low that loss of carrier lock is likely to occur.

The precorrelation bandwidth for these simulations was set at 8.184 MHz (4 times the C/A code bandwidth), using a 5th order Butterworth filter.

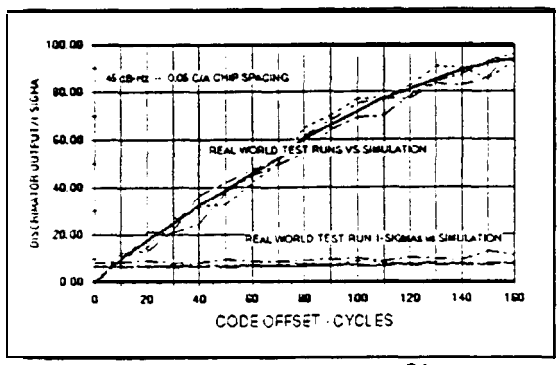

Figure 13 - EL Discriminator Simulated Versus Test Results

The slope of the discriminator at zero code error is the gain of the discriminator that must be accounted for when computing tracking loop gains. Note that in Figure 12, the slope is essentially constant at all the evaluated C/N_0 values, which is the property of the normalized discriminator. The theoretical wideband discriminator slope is simply the evaluation of Equation 4 divided by τ at $\tau = 0$, yielding:

$$\frac{E(d\tau)}{\tau} = \frac{4}{2\text{-}d} \qquad (5)$$

Thus, for a d of 1 chip, the gain is 4, while for a d of 0.05 chip, the gain is 2.0513. However, for this narrow spacing, the gain will be affected significantly because of bandlimiting.

Simulated Versus Test Performance Close-in expected discriminator output and its one sigma value is plotted in Figure 13, along with the same for three real-world test runs. In the case of the test runs, the discriminator output was sampled while controlling the open loop code offset with respect to the carrier phase after achieving steady state tracking. Note the agreement between the simulation and the test results. The test results exhibit the effects of precorrelation SAW IF bandpass filter response ripple.

The slope (or gain) of the EL discriminator as a function of correlator spacing is presented in Figure 14 for three cases: theoretical wideband, simulated bandlimited, and test results. Note the bandlimiting effects for narrow spacing. However, the simulated case and the test results agree very well.

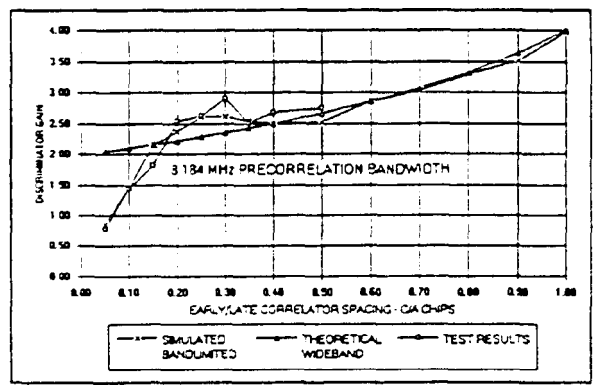

Figure 14 - EL Discriminator Gain

DLL Tracking Loop Analysis

The standard deviation of the pseudorange observables (σ_τ) can be estimated from the discriminator output standard deviation (Od) plotted in Figure 14 as follows:

$$\sigma_\tau = \frac{\sqrt{2B_L T}}{G_d}\sigma_d \qquad (6)$$

where Gd is the gain of the discriminator illustrated in Figure 14. For example, for a loop bandwidth of 1/30 Hz, the resulting σ_τ is approximately 0.3 cycles using the data from Figure 13.

Test Results

The accuracy of the pseudorange measurements were verified by collecting range and carrier phase data from two receivers over a zero base line (common antenna). Figure 15 shows the double differences of the raw pseudoranges. Notice that the standard deviation of the double difference range was 0.12 m. This translates to a single pseudorange standard deviation of 6

cm! This result far exceeds our design goal of 10 cm code phase measurement accuracy, and facilitates the establishment of the integer ambiguity of the carrier phase.

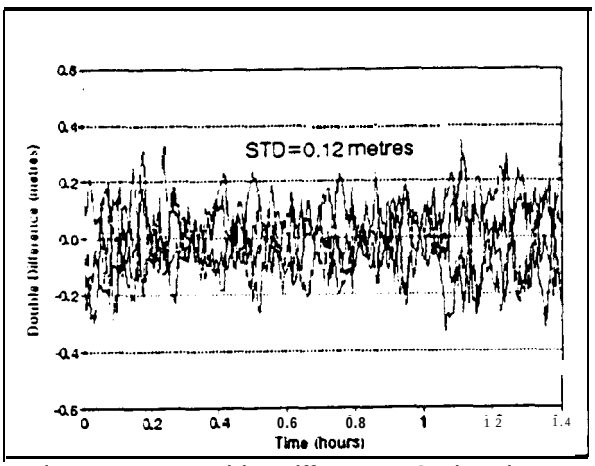

Figure 15 - Double Difference Code Phase Accuracy On Zero Length Baseline

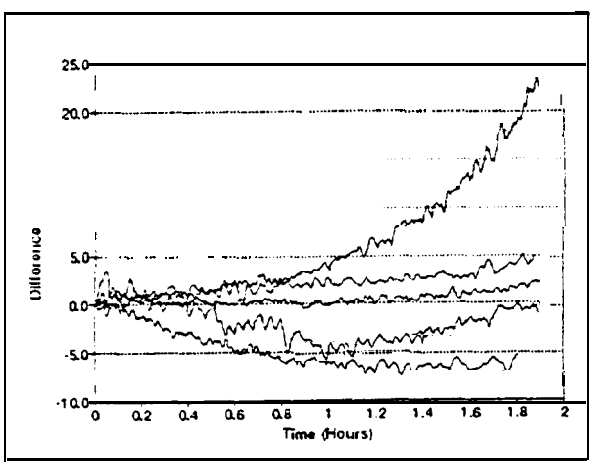

Figure 16 - Carrier-Code Phase Divergence On Five Parallel Channels

One of the side benefits of accurate pseudorange measurements is the code/carrier phase divergence observable. The divergence measurement can be seen in Figure 16. This measurement can be used to accurately model relative changes in the ionosphere and determine code phase multipath effects. In our receiver, the DLL simply tracks the difference between the carrier and code phases. Thus, this observable is simply the accumulation of all DLL loop updates. For more results and analysis using data collected by this receiver, consult [Erickson et al, 1991].

Summary and Conclusions

The major features of the NovAtel GPS receiver design have been discussed with an emphasis on hardware. The major architectural attributes of the signal processing chip, which facilitates accurate C/A code tracking, were detailed. The signal processing theory was overviewed to illustrate the design and performance enhancements. Finally, actual C/A code tracking results were presented which verify the expected performance.

The unique design features of the receiver provide the following capabilities:

1) P code pseudorange measurement accuracies with a C/A code receiver,

2) single frequency relative ionospheric delay measurements, and

3) carrier phase cycle slip detection and correction using code phase.

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